UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/955,926	09/18/2001	Catherine Mallardeau	00-GR1-374	9396

23334 7590 03/29/2004

FLEIT, KAIN, GIBBONS, GUTMAN, BONGINI
& BIANCO P.L.
ONE BOCA COMMERCE CENTER
551 NORTHWEST 77TH STREET, SUITE 111
BOCA RATON, FL 33487

EXAMINER	
MAGEE, THOMAS J	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 03/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/955,926	MALLARDEAU ET AL.	
	Examiner	Art Unit	
	Thomas J. Magee	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23, and 30 -38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23 and 30-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawing Objections

1. The drawings are objected to under 37 CFR 1.83(b) because they fail to show the presence of a silicide layer within active areas of the device as described in the specification and claims. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. *MPEP 608.02(d)*. A proposed drawing correction is required in response to avoid abandonment.

Claim Rejections – 35 U.S.C. 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 35, 36, and 38 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Applicant refers parenthetically to the presence of a silicide at the junction or active area of the device in a two line sentence of an alternate embodiment (p.14, Specification) but does not provide an enabling description of how the silicide is formed in the invention and its relationship to the terminal metal.

Claim Rejections – 35 U.S.C. 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 2, 4 – 6, and 30 – 32 are rejected under 35 U.S.C. 102(e) as being anticipated by Deboer et al. (US 6,677,636 B2).

6. Regarding Claims 1, 2, 30, and 31, Deboer et al. disclose an integrated circuit having a plurality of active components (Col. 1, lines 29 – 32) including junctions formed in a substrate (Col. 4, lines 30 – 32) and at least one passive component (capacitor) situated (Col. 6, lines 38 – 39) (61) (Figure 5) above the active components, wherein, the integrated circuit comprises a first insulating layer (only) (34,36) separating the active components and a base (60) of the passive component, with the base contacting (at the edges) the upper surface of layer 36. Deboer et al. further disclose a metal terminal (39) wherein, the metal terminal is a single layer of metal extending from the junction area of an active component to the base of the passive component, providing electrical connection between the two and formed in the thickness of the first insulating layer (36) with the lower surface extending over a boundary of the junction of an active region.

7. Regarding Claim 4, Deboer et al. disclose (Col. 4, lines 42 – 50) that the thickness of the first insulating layer is greater than 0.3um, and the surface planarized and contact plugs (39) formed made of tungsten (Col. 4, lines 60 – 64).

8. Regarding Claim 5 Deboer et al. disclose (Figure 5) the presence of a second insulating layer (44) above the first where the passive component is set into a cavity formed through out the thickness of the layer.

9. Regarding Claim 6, Deboer et al. disclose that the thickness of the second insulating layer (Col. 5, lines 11 – 13) is between about 0.8 and 2.0 um. Therefore, 2.01 um is about 2.0 um, and the disclosure by Deboer et al. is consistent with the claim of the instant application, wherein the thickness is greater than 2.0 um.

10. Regarding Claim 32, Deboer et al. disclose (Figure 5) areas of dielectric material (bottom of figure, right and left hand sides with "bird's beak") that separate active areas of the circuit, wherein, part of the lower surface (39) of the metal terminal contacts the dielectric material.

Claim Rejections – 35 U.S.C. 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Deboer et al., as applied to Claims 1, 2, 4, 5, 30, and 31, in view of Maeda (US 6,358,820 B1).

13. Regarding Claim 3, Deboer et al. do not disclose that the passive component is an inductor. However, Maeda discloses (Col. 7, lines 3 – 17) an inductor (20) (Figure 1) within an insulating film (silicon oxide) formed on a first insulating structure (Figure 15) and electrically connected to a junction (14a1) through interconnects. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Deboer et al. and Maeda to provide a means of incorporating an inductor on an insulating film above an active region with reduced parasitic capacitance in an integrated circuit.

14. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Deboer et al. in view of Maeda.

15. Regarding Claim 10, as discussed above, Deboer et al. do not disclose the presence of an inductor. Maeda discloses an inductor formed on an insulator and connected to inter-connects. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Deboer et al. and Maeda to provide a means of incorporating an inductor on an insulating film above an active region with reduced parasitic capacitance in an integrated circuit.

16. Claims 7 – 23, 33, 34, and 37 are rejected under Deboer et al. in view of Abernathey et al. (US 5,453,400).

17. Regarding Claims 7 and 34, Deboer et al. disclose (Figure 5) an integrated circuit containing a plurality of transistors, passive components, and local metal interconnections formed within the first insulating layer atop transistors of the integrated circuit, wherein the integrated circuit comprises a first metal terminal (41) passing completely through the first insulating layer (36) having an upper surface that contacts a second stage of contact between the active area and the first level of interconnection, wherein the metal terminal consists of a single layer of metal . Deboer et al. further disclose a second metal terminal (39) passing completely through the thickness of the first insulating layer, wherein the second metal vertically connects one active area of the integrated circuit to a passive component that directly contacts the upper surface of the insulating layer.

Deboer et al. do not disclose the presence of a third single metal passing completely through the thickness of the first insulating layer, wherein the third metal horizontally connects two active areas of the integrated circuit. Abernathey et al. disclose a single metal (tungsten) layer (34) (Figure 2B) connecting two active (source/drain) areas of an integrated circuit (Col. 4, lines 40 – 47). It would have then been obvious to one of ordinary skill in the art at the time of the invention to combine the procedures of Abernathey et al. in Deboer et al. to form a plug structure within an insulating layer to locally interconnect active circuit features.

18. Regarding Claims 8, 15, and 20, Deboer et al. disclose (Figure 5) that the second metal terminal has a lower surface that contacts the junction of one of the transistors of the integrated circuit such that the lower surface extends over a boundary of the junction.

19. Regarding Claim 9, Deboer et al. disclose (Col. 6, lines 38 – 40) (Figure 5) that the passive components include capacitors.

20. Regarding Claim 11, Deboer et al. disclose (Col. 4, lines 42 – 50) that the thickness of the first insulating layer is greater than 0.3um, and the surface planarized and contact plugs (39) formed made of tungsten (Col. 4, lines 60 – 64).

21. Regarding Claim 12, Deboer et al. disclose (Figure 5) the presence of a second insulating layer (44) above the first and resting on the first insulating layer, where the passive component is set into a cavity formed through out the thickness of the layer.

22. Regarding Claims 14, 18, 19, and 23, Deboer et al. disclose a integrated circuit comprising an onboard memory plane of DRAM cells in a matrix, each containing a control transistor and a storage capacitor (Col. 1, lines 29 – 40) with a plurality of transistors, passive components, and first level local metal interconnections above storage capacitors, a first insulating layer (36) separating MOS transistors and base of storage capacitors, a level of local connections, including three metal terminals (39,41) (Figure 5), each opening onto each side of the first insulating layer, a first metal terminal

forming a first stage of contact between an active area of the circuit and first level of interconnection (51), having an upper surface that contacts a second stage of contact between the active area and the first level of interconnection, wherein the metal terminal (tungsten) (Col. 4, lines 61 – 62) consists of a single layer of metal. Deboer et al. further disclose a second metal terminal (39) (tungsten) passing completely through the thickness of the first insulating layer, wherein the second metal vertically connects one active area of the integrated circuit to a passive component that directly contacts the upper surface of the insulating layer.

Deboer et al. do not disclose the presence of a third single metal passing completely through the thickness of the first insulating layer, wherein the third metal horizontally connects two active areas of the integrated circuit. Abernathey et al. disclose a single metal (tungsten) layer (34) (Figure 2B)connecting two active (source/drain) areas of an integrated circuit (Col. 4, lines 40 – 47). It would have then been obvious to one of ordinary skill in the art at the time of the invention to combine the procedures of Abernathey et al. in Deboer et al. to form a plug structure within an insulating layer to locally interconnect active circuit features.

23. Regarding Claims 16 and 21, Deboer et al. disclose (Figures 4 and 5) a second insulating layer (44) above the first insulating layer (36), with a cavity passing through the entire thickness of the second insulating layer and opening onto the top surface of the second metal terminal (39), wherein one plate (Figure 4) of the storage capacitor carpets the bottom and inside flanks of the cavity.

24. Regarding Claims 17 and 22, Deboer et al. disclose (Figure 8) a third insulating layer (54) above the second insulating layer (44) with a contact opening (68) passing through the second and third insulating layer and opening onto the top surface of the first metal terminal (41).

25. Regarding Claim 33, Deboer et al. disclose (Figure 5) that the first insulating layer (36) is a single layer and the only insulating layer provided between the transistors and a base of the passive component.

26. Regarding Claim 37, Deboer et al. disclose (Figure 5) that the second metal terminal (39) has an upper surface that contacts the passive component and consists of a single layer of metal extending from the junction to the passive component.

Response to Arguments

27. Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusions

28. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(571) 272**

1658. The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Eddie Lee**, can be reached on **(571) 272-1732.** The fax number for the organization where this application or proceeding is assigned is **(703) 872-9306.**

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Thomas Magee
March 12, 2004